IN THE CLAIMS:

1-15. (Canceled)

16. (Currently Amended): A wafer for testing by a testing device, the wafer comprising:

a plurality of integrated circuits, wherein each integrated circuit includes testing circuitry;

a network of signal paths on the wafer, wherein the network of signal paths connects the plurality of integrated circuits to two or more connection points;

a current mirror; and

a plurality of transistors,

wherein in response to the testing device being connected to the connection points, the testing circuitry performs a test on the plurality of integrated circuits concurrently, [[and]]

wherein each integrated circuit includes at least one visible component having an appearance and wherein the at least one visible component permanently changes its appearance in response to failing the test,

wherein the at least one visible component includes at least one diode-connected transistor,

wherein the current mirror receives a high current and passes an equal amount of current to each of the plurality of transistors, and

wherein the plurality of transistors, responsive to an input signal, pass current to the diode-connected transistor, causing the diode-connected transistor to burn up and leave a visible mark.

17-34. (Canceled)

35. (Previously Presented): A method of testing a circuit, comprising:

applying at least one signal to testing circuitry;

in response to a determination that the circuit is defective, modifying a visible circuit component in the circuit to have a different appearance, wherein modifying the visible circuit component includes causing the visible circuit component to overheat.

36-39. (Canceled)

40. (Previously Presented): The wafer of claim 16, wherein the network of signal paths includes a power supply signal path.

41. (Previously Presented): The wafer of claim 16, wherein the network of signal paths includes a clock signal path.

42. (Previously Presented): The wafer of claim 16, wherein the network of signal paths includes a control signal path.

43. (Previously Presented): The wafer of claim 16, wherein the network of signal paths is located on a scroll line.